

# Hyungmin Cho, Ph.D.

Assistant Professor

Department of Software  
College of Computing  
Sungkyunkwan University, Korea

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## EDUCATION

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| Apr. 2010 – Aug. 2015 | Ph.D. in Electrical Engineering<br>Stanford University, Stanford, CA<br>Research Advisor: Prof. Subhasish Mitra<br>Thesis: “System-level Effects of Soft Errors” |
| Sep. 2008 – Mar. 2010 | M.S. in Electrical Engineering<br>Stanford University, Stanford, CA<br>Research Advisor: Prof. Subhasish Mitra   |
| Mar. 2001 – Feb. 2005 | B.S. in Computer Science and Engineering<br>Seoul National University, Seoul, South Korea<br>Honors: Summa Cum Laude (GPA: 4.04/4.3)                             |

## RESEARCH INTERESTS

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- Computer architecture
  - Error resilient robust systems architecture
  - Processor security
- Efficient deep-learning architecture
  - FPGA-based deep neural network acceleration
  - Architecture design for reinforcement learning
  - GPU scheduling techniques
- Hardware reliability
  - Application-level error resilience techniques
  - Soft error mitigation techniques

## EXPERIENCES

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- Sep. 2019 – Present      Department of Software, Sungkyunkwan University  
Assistant Professor
- Mar. 2017 – Aug. 2019    Department of Computer Engineering, Hongik University  
Assistant Professor
- Oct. 2015 – Feb. 2017    Intel Corporation  
Santa Clara, CA  
Research Scientist, Microarchitecture Research Lab
- Apr. 2009 – Aug. 2015    Robust Systems Group, Stanford University  
Research Assistant
- Robust hardware design
  - Error-resilient software execution models
  - System-level soft error analysis
- Jun. 2011 – Sep. 2011    Texas Instruments Inc.  
Dallas, TX  
Intern, Signal Processing VLSI Group
- Jun. 2009 – Sep. 2009    NEC Laboratories America, Inc.  
Princeton, NJ  
Intern, Computer Systems Architecture group
- Feb. 2005 – May 2008    Bluebird Inc.  
Seoul, South Korea  
System Programmer, Platform development team
- Oct. 2006 – Apr. 2007    Advanced Compiler Research Lab, Seoul National University  
Research Intern
- Linker level data scratch pad memory allocation mechanism for ARM based system

## AWARD & SCHOLARSHIP

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- Aug. 2007      Fellowship for graduate studies from the Korea Foundation for Advanced Studies (KFAS)
- Feb. 2005      Graduated with Summa Cum Laude honors, Seoul National University
- Sep. 2004      Full scholarship from Computer Science and Engineering department, Seoul National University

## Research Grants

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- High-Efficiency Adaptive Architecture for Deep Neural Network Training (고효율 적응형 딥러닝 학습 플랫폼), PI (연구책임자), Ministry of Science and ICT (과학기술정보통신부/한국연구재단), 875,000,000 KRW, Jun. 2019 – Feb. 2021.
- Research on CPU Vulnerability Detection and Validation (컴퓨터 프로세서의 구조적 보안 취약점 검증 및 공격 탐지 대응), Co-PI (참여기관 연구책임자), Ministry of Science and ICT (과학기술정보통신부/정보통신기획평가원), 5,600,000,000 KRW, Apr. 2019 – Dec. 2022.
- Efficient Neural Network Computation Platform for Internet of Things (사물인터넷 환경에서의 효율적인 인공지능 계산 플랫폼 연구), PI (연구책임자), Ministry of Science, ICT and Future Planning (미래창조과학부/한국연구재단), 90,000,000 KRW, Mar. 2017 – Feb. 2020.

## COURSES TAUGHT

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- Undergrad Courses at Hongik University
  - **101510**: Computer Architecture
  - **004174**: Introduction to Computer Science and Engineering
  - **101408**: Assembly Programming Language
  - **101711**: Embedded Systems
- Graduate Courses at Hongik University
  - **1072025**: Advanced Topics in Microprocessors

## SKILLS

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Hardware design	System Verilog, VHDL, FPGA, VLSI back-end flow
Software	C, C++, Objective-C, Python, Perl, Matlab, TensorFlow, OpenCL, CUDA

## CONFERENCE PUBLICATIONS

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- **Hyungmin Cho**, Pyeongseok Oh, Jiyoung Park, Wookeun Jung, and Jaejin Lee, “FA3C: FPGA-Accelerated Deep Reinforcement Learning,” *Proc. International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Providence, RI, USA, April 2019 (Acceptance rate: 21.1%)
- Eric Cheng, Jacob Abraham, Pradip Bose, Alper Buyuktosunoglu, Keith Campbell, Deming Chen, Cheng-Yong Cher, **Hyungmin Cho**, Binh Le, Klas Lilja, Shahrzad Mirkhani, Kevin Skadron, Mircea Stan, Lukasz Szafaryn, Christos Vezyrtzis, and Subhasish Mitra, “Cross-layer resilience in low-voltage digital systems: key insights,” *Proc. International Conference on Computer Design (ICCD)*. Boston, MA, USA, Nov. 2017 (Invited).
- E. Cheng, S. Mirkhani, L. Szafaryn, C.-Y. Cher, **Hyungmin Cho**, K. Skadron, M. Stan, K. Lilja, J. Abraham, P. Bose and S. Mitra, “CLEAR: Cross-Layer Exploration for Architecting Resilience: Combining Hardware and Software Techniques To Tolerate Soft Errors in Processor Cores,” *Proc. Design Automation Conf. (DAC)*, Austin, TX, USA, June 2016 (Acceptance rate: 17%).
- **Hyungmin Cho**, C.-Y. Cher, T. Shepherd, and S. Mitra, “Understanding Soft Errors in Uncore Components,” *Proc. Design Automation Conf (DAC)*, San Francisco, CA, USA, June 2015 (Acceptance rate: 20.5%).
- S. Mitra, P. Bose, E. Cheng, **Hyungmin Cho**, R. Joshi, Y. M. Kim, C. R. Lefurgy, Y. Li, K. P. Rodbell, K. Skadron, J. Stathis and L. Szafaryn, “The Resilience Wall: Cross-Layer Solution Strategies,” *Proc. IEEE Intl. Symp. VLSI Technology, Systems and Applications and IEEE Intl. Symp. VLSI Design, Automation and Test*, Hsinchu, Taiwan, April 2014 (Invited).
- S. Mirkhani, **Hyungmin Cho**, S. Mitra, and J. A. Abraham, “Rethinking Error Injection for Effective Resilience,” *Proc. Asia and South Pacific Design Automation Conf. (ASPDAC)*, Jan. 2014 (Invited).
- **Hyungmin Cho**, S. Mirkhani, C.-Y. Cher, J. A. Abraham, and S. Mitra, “Quantitative Evaluation of Soft Error Injection Techniques for Robust System Design,” *Proc. Design Automation Conf. (DAC)*, Austin, TX, USA, June 2013 (Acceptance rate: 23%).
- L. Leem, **Hyungmin Cho**, H.-H. K. Lee, Y. M. Kim, Y. Li, and S. Mitra, “Cross-Layer Error Resilience for Robust Systems,” *Proc. Intl. Conf. Computer-Aided Design (ICCAD)*, Nov. 2010 (Invited).
- L. Leem, **Hyungmin Cho**, J. Bau, Q. A. Jacobson, S. Mitra, “ERSA: Error Resilient System Architecture for probabilistic applications,” *Proc. Design, Automation & Test in Europe (DATE)*, March 2010 (Acceptance rate: 25%).
- **Hyungmin Cho**, B. Egger, J. Lee, and H. Shin, “Dynamic Data Scratchpad Memory Management for a Memory Subsystem with an MMU,” *Proc. Languages, Compilers, and Tools for Embedded Systems (LCTES)*, June 2007.

## JOURNAL PUBLICATIONS

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- **Hyungmin Cho** and Kon-Woo Kwon, "Modeling Application-Level Soft Error Effects for Single-Event Multi-Bit Upsets," *IEEE Access*, vol. 7, 2019
- HyungGyoon Kim, **Hyungmin Cho**, and Changwoo Pyo, "GPU-based acceleration of the linear complexity test for random number generator testing," *Journal of Parallel and Distributed Computing*, vol. 128, 2019
- Eric Cheng, Shahrzad Mirkhani, Lukasz G Szafaryn, Chen-Yong Cher, **Hyungmin Cho**, Kevin Skadron, Mircea R Stan, Klas Lilja, Jacob A Abraham, Pradip Bose, Subhasish Mitra, "Tolerating soft errors in processor cores using clear (cross-layer exploration for architecting resilience)," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol.37, no.9, pp.1839-1852, Sept. 2018.
- **Hyungmin Cho**, "ASIC-Resistance of Multi-Hash Proof-of-Work Mechanisms for Blockchain Consensus Protocols," *IEEE Access*, vol. 6, 2018
- **Hyungmin Cho**, "Impact of Microarchitectural Differences of RISC-V Processor Cores on Soft Error Effects," *IEEE Access*, vol. 6, 2018
- **Hyungmin Cho**, E. Cheng, T. Shepherd, C.-Y. Cher, and S. Mitra, "System-level Effects of Soft Errors in Uncore Components," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol.36, no.7, pp.1497-1510, Sept. 2017.
- S. M. S. Yazdi, **Hyungmin Cho**, L. Dolecek, "Gallager B decoder on noisy hardware," *IEEE Transactions on Communications*, vol.61, no.5, pp.1660-1673, May 2013.
- **Hyungmin Cho**, L. Leem, and S. Mitra, "ERSA: Error Resilient System Architecture for Probabilistic Applications," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol.31, no.4, pp.546-558, April 2012.
- S. Mitra, **Hyungmin Cho**, T. Hong, Y. M. Kim, H.-H. K. Lee, L. Leem, Y. Li, D. Lin, E. Mintarno, S.-B., Park, N. Patil, H. Wei and J. Zhang, "Robust System Design," *IPSJ Trans. System LSI Design Methodology*, 2011 (Invited)

## PATENTS

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- S. Chakradhar, **Hyungmin Cho**, A. Raghunathan, "Cross-layer system architecture design," US Patent 8,762,794, June 2014.